

REMARKS

None of the claims have been amended or cancelled. Claims 1 and 2 are pending and under consideration. Claim 1 is the independent claim. No new matter is presented in this Amendment.

REJECTIONS UNDER 35 U.S.C. §102:

Claim 1 is rejected under 35 U.S.C. §102(e) as being anticipated by Ichikawa (U.S. Patent No. 5,901,159).

Applicants respectfully traverse this rejection for at least the following reasons.

Regarding the rejection of claim 1, it is noted that claim 1 recites a recording/reproducing apparatus comprising; a data scrambler having a random data generator for generating random data in a cycle of 32 KB in order to scramble data having a structure of 2 KB for a sector or a data frame and 64 KB for an ECC block.

The Office Action relies on Ichikawa for the teachings of claim 1 and in particular cites column 15, lines 1-30 and column 14, lines 50-67 for such teachings.

However, a careful review of Ichikawa and of the cited passages reveals that Ichikawa does not in fact teach or suggest the novel features recited in independent claim 1, as discussed below.

Ichikawa discloses an apparatus and method for decoding and error correcting a coded digital video signal having error correction data added thereto and reproduced from a record medium, e.g., a compact disk (column 1, lines 4-9).

The data reproducing apparatus 40 includes a pickup device 3 which provides a laser beam onto optical disk 2 to reproduce the data recorded thereon. Pickup device 3 supplies a reproduced signal S1 to a demodulating circuit 6 included in a demodulating system 35 which is controlled by a system controller 4. The reproduced signal S1 is demodulated and supplied to sector detection circuit 7 which detects addresses from each sector therein and supplies the addresses to ring buffer control circuit 11 and also supplies the data included in the signal to an ECC (error correction code) circuit 50. ECC circuit 50 detects and corrects errors. Sector detection circuit 7 detects new sectors in the reproduced signal, but if a sector number or address is not detected or if continuous detection does not occur, a sector number error signal is

supplied via ring buffer control circuit 11 to a track jump determination circuit 9. Similarly, an error signal is supplied via system controller 4 to track jump determination circuit 9 if ECC circuit 50 detects an uncorrectable error in the signal (column 6, line 65 - column 7, line 23).

Ichikawa further discloses the data structure of a sector and how the main data of the sector is scrambled. In particular, Ichikawa discloses in FIG. 25 the data structure of a sector without the PI and PO parity data. The sector includes a 4 byte ID code (i.e., a sector number), a two-byte error-detecting code for the ID code (IED), 6 bytes of reserved data (RSV), scrambled main data, and 4 bytes of EDC (error-detecting code). Sixteen sectors are combined with PI and PO data, and frame synchronization codes FS are added, such as shown in FIG. 22. The frame synchronization codes are represented as SYx (x=0, 1, 2, . . . 7), such as shown in FIG. 24, and since one ECC block is comprised of 16 sectors, the lower 4 bits of the physical sector address is set from 0000 to 1111, where the lower 4 bits of the physical address of the first sector of the ECC block is 0000 (column 14, lines 53-67). The main data of the sector shown in FIG. 25 is scrambled by exclusively logically adding together the main data with scramble data generated using as the initial value a value specified by the lower 4 to 7 bits of the physical sector address (column 15, lines 1-5).

Accordingly, Ichikawa simply discloses an apparatus for reading data recorded on a storage medium and a method of scrambling the main data of a sector by adding the main data with scramble data and generating the scramble data by using the lower 4 to 7 bits of the physical sector address.

Ichikawa does not teach or suggest that the apparatus includes a random data generator for generating random data using a 32KB cycle nor does Ichikawa teach or suggest the sizes of the ECC block, the sector and the data frames.

In particular, Ichikawa fails to teach or suggest that the scramble data has a structure of 2KB for a sector or a data frame and 64KB for an ECC block, as recited in independent claim 1.

Accordingly, Applicants respectfully assert that the rejection of claim 1 under 35 U.S.C. § 102(e) should be withdrawn because Ichikawa fails to teach or suggest each feature of independent claim 1.

REJECTIONS UNDER 35 U.S.C. §103:

Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Ichikawa, and

further in view of Unno (U.S. Patent No.6,577,647).

Initially it is noted that claim 2 depends from claim 1, and as noted above, Ichikawa fails to teach or suggest the novel features of independent claim 1.

Unno on the other hand is relied upon solely for a teaching of a random data generator and thus fails to cure the deficiencies of Ichikawa.

Accordingly, Applicants respectfully assert that the rejection of claim 2 under 35 U.S.C. §103(a) should be withdrawn because neither Ichikawa nor Unno, whether taken singly or combined teach or suggest each feature of independent claim 1, from which claim 2 depends, and because claim 2 includes additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claim 2 also distinguishes over the prior art.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

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